WHAT IS CLAIMED IS:

1. A semiconductor circuit comprising:

a first transistor having:

a first semiconductor region;

spaced-apart source and drain regions formed in the first semiconductor region;

a first channel defined between the source and drain regions, the first channel having a first channel length and a first dopant concentration;

a layer of first gate oxide formed over the first channel, the layer of first gate oxide having a thickness; and

a gate formed over the layer of first gate oxide;

the first transistor conducting more than a leakage current when the gate, the source, and the first semiconductor region are connected to a same potential;

a second transistor having:

a second semiconductor region;

spaced-apart source and drain regions formed in the second semiconductor region;

a second channel defined between the source and drain regions formed in the second semiconductor material, the second channel having a second channel length and a second dopant concentration;

a layer of second gate oxide formed over the second channel, the layer of second gate oxide having a thickness, the thickness of the layer of first gate oxide being substantially less than the thickness of the layer of second gate oxide; and

a gate formed over the layer of second gate oxide;

the second transistor being substantially non-conductive when the gate of the second transistor, the source of the second transistor, and the second semiconductor region are connected to a same potential, the first channel

length being approximately 30 percent to 80 percent as long as the second channel length.

2. The circuit of claim 1 wherein the first dopant concentration is greater than the second dopant concentration.

3. The circuit of claim 1 and further comprising a third transistor formed in the semiconductor material, the third transistor having a third channel and a layer of third gate oxide formed over the third channel, the third channel having a third channel length and a third dopant concentration, the layer of third gate oxide having a thickness, the third transistor being substantially non-conductive when zero volts are applied to the gate, the thickness of the layer of third gate oxide being substantially equal to the thickness of the layer of first gate oxide.

4. The circuit of claim 3 wherein the first dopant concentration is substantially equal to a sum of the second dopant concentration and a dopant concentration implanted into the third channel.

5. The circuit of claim 4 wherein the second and third transistors have source and drain regions of the same conductivity type, and the first transistor has source and drain regions of an opposite conductivity type.

6. The circuit of claim 4 wherein the first and third transistors have source and drain regions of the same conductivity type, and the second transistor has source and drain regions of an opposite conductivity type.

7. The circuit of claim 1 wherein the source and drain regions of the second transistor are spaced apart from the source and drain regions of the first transistor.

8. The circuit of claim 1 wherein the gate formed over the layer of second gate oxide does not contact the source or drain region of the second transistor.